REMARKS

Claims 1-19 are pending in the present application and are rejected. Claims 15-19 are withdrawn. Claims 1-4, 7-8, 11-12 and 14 are herein amended. No new matter has been entered.

Claim Rejection - 35 U.S.C. 102

Claims 1-12 are rejected under 35 U.S.C. 102(a) as being anticipated by Yamamoto (U.S. Publication No. 2002/0153579).

Applicants herein amend the claims to more clearly define the invention. Thereafter, Applicants respectfully disagree with the rejection, because not all of the claimed limitations are taught or suggested by the cited reference.

Applicants note that Yamamoto discloses a semiconductor device comprising a first dielectric film 3 formed on a silicon substrate 1, a second dielectric film 4 formed on the first dielectric film 3, and a gate electrode 5a formed on the second dielectric film 4 (Fig. 1). In Yamamoto, the first dielectric film 3 is formed of Al_2O_3 and the second dielectric film 4 is formed of ZrO_2, Ta_2O_5, etc. Aluminum is a III group element, and Ta is a V group element.

On the other hand, the present invention is characterized in that a semiconductor substrate 6 is formed of a semiconductor (e.g., Si) containing a first element of a IV group element; and an intermediate layer 12 is formed of an oxide (e.g., AlTaSiO) containing the first element (e.g., Si) of the IV group element and a second element (e.g., Ta) which is either of a III group element or a V group element; and an insulation film 14 is formed of an oxide (e.g., Al_2O_3) of a third element (e.g., Al) which is the other of the III group element and the V group element (see

attached paper). That is, in the present invention, the intermediate layer 12 contains not only III or V group element but also a IV group element that is the same material of the semiconductor substrate 6.

In the present invention, since the oxide (e.g., AlTaSiO) of the intermediate layer 12 contains not only III or V group element (e.g., Ta) but also IV group element (e.g., Si) that is the same material of the semiconductor substrate 6, an oxide (e.g., SiO_2) of the IV group element is formed at an interface of the semiconductor substrate 6 and the intermediate layer 12. Because the oxide (e.g., SiO_2) of the IV group element is formed at the interface of the semiconductor substrate and the intermediate layer (e.g., AlTaSiO), it is possible to reduce the surface state density at the interface of the semiconductor substrate 6 and the intermediate layer 12. Since the surface state density can be decreased, it is possible to decrease a leak current.

In the present invention, since the intermediate layer (AlTaSiO) 12 contains the second element which is either of the III group element or the V group element, and an insulation film 14 is formed of the oxide (e.g., Al_2O_3) of the third element which is the other of the III group element and the V group element, dangling bonds of the insulation film 14 caused by the third element (e.g., Al) are reduced by the second element (e.g., Ta) of the intermediate layer 12. Since the dangling bonds can be decreased, it is possible to reduce the shift of the flat band voltage.

On the other hand, in Yamamoto, the first dielectric film 3 does not contain the IV group element that is the same material of the silicon substrate 1 (see attached paper). In Yamamoto, the first dielectric film 3 is formed in order to form the second dielectric film 4 with uniform

thickness. In Yamamoto, the first dielectric film 3 functions as a seed layer when the second dielectric film 4 is formed. Further in Yamamoto, since the first dielectric film 3 of Al_2O_3 is formed directly on the silicon substrate 1, the surface state density is large and the flat band voltage shift is large. Yamamoto neither discloses nor suggests such feature of the present invention. Accordingly, the present invention is patentably distinguished from Yamamoto.

Claim Rejection - 35 U.S.C. 103

Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto in view of U.S. Patent No. 6,013,553 to Wallace et al., which discloses a semiconductor device comprising a zirconium oxynitride layer 36 formed over a substrate 20, and a conductive gate formed on the zirconium oxynitride layer 36.

Applicants respectfully disagree with this rejection because not all of the claimed limitations are taught or suggested by the cited reference. Applicants note that the zirconium oxynitride layer 36 does not correspond to the intermediate layer of the present invention. The zirconium oxynitride layer 36 of Wallace et al. is a gate insulation film; therefore, Wallace et al. is not relevant to the present invention. These references neither disclose nor suggest above-mentioned feature of the present invention.

In view of the aforementioned amendments and accompanying remarks, Applicants submit that that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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Attachment: Graphical Comparison of Present Invention and Cited Reference
Replacement Figure 5